

CLAIMS

- 1 1. (Currently amended) A method of fabricating a CMOS device comprising the steps
2 of:
 - 3 (a) forming a gate dielectric on a semiconductor substrate that can be sectioned
4 into a p-well region for forming an NMOSFET and a n-well region for
5 creating PMOSFET;
 - 6 (b) forming ~~[[a]]~~ an aluminum nitride buffer layer material over the gate dielectric;
 - 7 (c) depositing a first metal on the buffer layer;
 - 8 (d) selectively etching the first metal with a first etchant so that the buffer layer is
9 exposed on one of said p-well and n-well regions;
 - 10 (e) depositing a second metal on both the exposed buffer layer and the remaining
11 first metal;
 - 12 (f) removing said first metal and said second metal and said buffer layer in
13 selected areas so as to form a PMOSFET gate electrode and an NMOSFET
14 gate electrode of said CMOS device; and
 - 15 (g) annealing remaining portions of said first metal and said second metal and said
16 buffer layer to consume said portions of said buffer layer by reacting with said
17 first metal and said second metal to form first and second conductive alloys
18 with first and second work functions respectively.
- 1 2. (Original) A method as recited in claim 1 wherein said buffer layer material is
2 selected to have a resistance to said first etchant for protecting said gate dielectric
3 from said first etchant.
3. (Cancelled)

- 1 4. (Currently amended) A method as recited in claim [[3]] 1 wherein said buffer layer
2 has a buffer layer thickness less than 20nm.
- 1 5. (Original) A method as recited in claim 1 wherein said first etchant is a wet chemical
2 solution including a mixture of sulfuric acid and hydrogen peroxide.
- 1 6. (Original) A method as recited in claim 1 wherein said first etchant is a wet chemical
2 solution including a mixture of hydrofluoric acid and hydrogen peroxide.
- 1 7. (Original) A method as recited in claim 1 wherein said annealing is done at a
2 temperature in excess of 400°C.
- 1 8. (Original) A method as recited in claim 1 wherein said first metal is hafnium and said
2 second metal is tantalum.
- 1 9. (Original) A method as recited in claim 1 wherein said forming a buffer layer
2 material includes a process selected from the group consisting of physical vapor
3 deposition (PVD), chemical vapor deposition (CVD) and atomic layer deposition
4 (ALD).
- 1 10. (Currently amended) A method as recited in claim [[3]] 1 wherein a composition
2 ratio of ~~said aluminum to said nitrogen~~ the aluminum nitride is selected to achieve
3 desired work functions of said metal alloys.
- 1 11. (Currently amended) A method of determining a work function of a metal gate
2 electrode comprising:
3 determining a desired work function of a metal gate electrode including
4 (a) depositing [[a]] an aluminum nitride buffer layer material on a gate dielectric;
5 (b) depositing a metal on said buffer layer material; and

6 (c) annealing said buffer layer and said metal to cause said buffer material and
7 said metal to react and form an alloy having the desired work function.

12. (Cancelled)

1 13. (Currently amended) A method as recited in claim 42 ~~11~~ wherein a composition ratio
2 of ~~said-aluminum-and-said-nitrogen~~ the aluminum nitride is selected to achieve a
3 desired said work function.

1 14. (Currently amended) A method as recited in claim ~~[[3]]~~ 1 wherein the first metal and
2 second metal are selected from the group consisting of titanium (Ti), hafnium (Hf)
3 and tantalum (Ta).

1 15. (Currently amended) A method as recited in claim ~~[[3]]~~ 1 wherein the first metal and
2 second metal have an electronegativity of less than 1.34 ~~Ev~~.

1 16. (Currently amended) A metal gate for CMOS applications, wherein the contact area
2 between said metal gate and adjacent metal gate dielectric is comprised of an alloy
3 formed from ~~AlN~~, aluminum nitride and a metal whose electronegativity is less than
4 1.4.

1 17. (Original) A metal gate as in Claim 16, where the metal is Hf, and the alloy has a
2 work function of approximately 4.4Ev, appropriate for NMOS.

1 18. (Original) A metal gate as in Claim 16, where the metal is Ta, and the alloy has a
2 work function of approximately 4.9Ev, appropriate for PMOS.